TRANSMITTAL OF APPEAL BRIEF

Docket No.
SON-1976

In re Application of: Yuji Murayama, et al

Application No.	Filing Date	Examiner	Group Art Unit
09/739,318	December 19, 2000	E. Labaze	2876

Invention: PORTABLE ELECTRONIC APPARATUS, IC CARD AND READER/WRITER

TO THE COMMISSIONER OF PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed: March 4, 2003 .

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Dated: May 5, 2003

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Patent Application of

Yuji MURAYAMA et al. Art Unit: **2876**

Serial No. **09/739,318** Examiner: E. Labaze

Filed: December 19, 2000

For: PORTABLE ELECTRONIC APPARATUS, IC CARD AND READER/WRITER

APPEAL BRIEF

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an Appeal Brief under Rule 192 appealing the final decision of the Examiner dated November 7, 2002 (Paper No. 14). Each of the topics required by Rule 192 is presented herewith and is labeled appropriately.

I. Real Party In Interest

Sony Corporation of Tokyo, Japan ("Sony") is the real party in interest of the present application. An assignment of all rights in the present application to Sony was executed by the inventor and recorded by the U.S. Patent and Trademark Office at **reel 011865, frame 0206.**

II. Related Appeals And Interferences

There are no appeals or interferences related to the present application of which Appellant is aware.

III. Status of Claims

Claims 1-12 were originally filed and are pending in this application.

The Request for Reconsideration of September 24, 2002 canceled claims 1-12 and added claims 13-37.

The Request for Reconsideration of January 7, 2003 includes a proposed amendment to the claims. The Advisory Action of February 10, 2003 indicates that the proposed amendment will be entered for the purposes of appeal.

An Amendment After Final Rejection Under 37 C.F.R. § 1.116 has been filed concurrently with the Appeal Brief. Assuming entry of the Request for Reconsideration of January 7, 2003 and the Amendment After Final Rejection Under 37 C.F.R. § 1.116, appellant hereby appeals the final rejection of claims 13-37, which are presented in the Appendix.

IV. Status of Amendments

The Request for Reconsideration filed on January 7, 2003 includes a proposed amendment to the claims. The Advisory Action of February 10, 2003 indicates that the proposed amendment will be entered for the purposes of appeal.

An Amendment After Final Rejection Under 37 C.F.R. § 1.116 has been filed concurrently with the Appeal Brief, which has not been acted upon by the Examiner.

Assuming entry of the Amendment After Final Rejection Under 37 C.F.R. § 1.116, appellant hereby appeals the final rejection of claims 13-37, which are presented in the Appendix.

V. Summary of the Invention

The present invention relates to a portable electronic apparatus, an IC card and a reader/writer.

Described within figures 1-5 is a clock generation circuit 25. The clock generation circuit 25 uses a received signal S2,S3 to generate a clock signal CK and a sampling signal D2,D3, wherein received data is the information transmitted to the

portable electronic apparatus by way of the received signal S2,S3.

A decoder decodes a plurality of logic levels to generate the received data. As shown within figure 2, the sampling signal D2,D3 has a plurality of pulses during each cycle of the clock signal. A plurality of logic levels are generated during each cycle of clock signal. A logic level of the plurality of logic levels is the signal level of the received signal when sampled by a pulse of the plurality of pulses.

Described within figures 6-10 is a clock generation circuit 25 that uses a received signal S2,S3 to generate a clock signal CK, wherein the received data is the information transmitted to by way of the received signal S2,S3.

A correlation value detection circuit 32 compares the phase of the clock signal CK to the phase of the received signal S2,S3 to generate a correlation value signal. As shown within figures 7-9, the correlation value signal trends in a first direction when the clock signal CK is in phase with the received signal and trends in a direction opposite to the first direction when the clock signal CK is out of phase with the received signal S2,S3.

A determination circuit 33 uses the correlation value signal to generate the received data.

VI. References of Record

In the final rejection of November 7, 2002, the Examiner relied upon the following art:

U.S. Patent No. 5,850,187 to Carrender et al. (Carrender);

U.S. Patent No. 5,418,353 to Katayama et al. (Katayama);

U.S. Patent No. 5,010,237 issued to Kawana;

U.S. Patent No. 5,574,754 to Kurihara et al. (Kurihara).

VII. Issues

The issues presented for consideration in this appeal are as follows:

Whether the Examiner erred in rejecting claims 13-25 under 35 U.S.C. §103 as allegedly being obvious over Carrender in view of Katayama and Kawana.

Whether the Examiner erred in rejecting claims 26-37 under 35 U.S.C. §103 as allegedly being obvious over Carrender in

view of Kurihara.

These issues will be discussed hereinbelow.

VIII. Grouping of Claims

For purposes of the issues presented by this appeal:

Claim 13, 16, 17 stand or fall together.

Claim 14 stands or falls separately.

Claim 15 stands or falls separately.

Claim 18, 21 stand or fall together.

Claim 19 stands or falls separately.

Claim 20 stands or falls separately.

Claim 22, 25 stand or fall together.

Claim 23 stands or falls separately.

Claim 24 stands or falls separately.

Claim 26 stands or falls separately.

Claim 27 stands or falls separately.

Claim 28 stands or falls separately.

Claim 29 stands or falls separately.

Claim 30 stands or falls separately.

Claim 31 stands or falls separately.

Claim 33 stands or falls separately.

Claim 32 stands or falls separately.

Claim 34 stands or falls separately.

Claim 35 stands or falls separately.

Claim 36 stands or falls separately.

Claim 37 stands or falls separately.

The arguments set forth in the following section provide reasons why these groups are considered patentable, 37 C.F.R. §1.192 (c)(7).

IX. Arguments

In the Final Office Action of November 7, 2002:

The Examiner rejected claims 13-25 under 35 U.S.C. §103 as allegedly being obvious over Carrender in view of Katayama and Kawana.

The Examiner rejected claims 26-37 under 35 U.S.C. §103 as allegedly being obvious over Carrender in view of Kurihara.

For at least the following reasons, Appellant submits that these rejections are both technically and legally unsound and should therefore be reversed.

General Matters

M.P.E.P. 707.07(f) states that "the importance of answering such arguments is illustrated by In re Herrmann, 261 F.2d 598, 120 USPQ 182 (CCPA 1958) where the applicant urged that the subject matter claimed produced new and useful results. The court noted that since applicant's statement of advantages was not questioned by the examiner or the Board of Appeals, it was constrained to accept the statement at face value and therefore found certain claims to be allowable. See also In re Soni, 54 F.3d 746, 751, 34 USPQ2d 1684, 1688 (Fed Cir. 1995) (Office failed to rebut applicant's argument)."

"The Patent and Trademark Office (PTO) has the burden of showing a prima facie case of obviousness." *In re Bell*, 26 USPQ2d 1529, 1530 (Fed. Cir. 1993). "In determining the propriety of the Patent Office case for prima facie obviousness, it is necessary to ascertain whether the prior art teachings would appear to be sufficient to one of ordinary skill in the art to suggest making the proposed substitution or other modification." *In re Taborsky*, 183 USPQ 50, 55 (CCPA 1974). Moreover, prima facie obviousness of a claimed invention is established "only by showing some objective teaching in the prior art or that knowledge generally

available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references." *In re Fine*, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

The Examiner erred in rejecting claims 13-25 under 35 U.S.C. §103 as allegedly being obvious over Carrender in view of Katayama and Kawana.

This rejection is respectfully traversed, at least for the following reasons.

Claim 13, 16, 17

Claim 13 and the claims dependent thereon are drawn to a portable electronic apparatus comprising:

> a clock generation circuit, the clock generation circuit using a received signal to generate a clock signal and a sampling signal,
>
> received data being the information transmitted to the portable electronic apparatus by way of the received signal,

the sampling signal having a plurality of pulses during each cycle of the clock signal,

a plurality of logic levels being generated during the each cycle of the clock signal,

a logic level of the plurality of logic levels being the signal level of the received signal when sampled by a pulse of the plurality of pulses; and

a decoder, the decoder decoding the plurality of logic levels to generate the received data.

Within claim 13 the clock generation circuit uses a received signal to generate a clock signal and a sampling signal. The sampling signal has a plurality of pulses during each cycle of the clock signal. A plurality of logic levels is generated during each cycle of the clock signal, and a logic level of the plurality of logic levels is the signal level of the received signal when sampled by a pulse of the plurality of pulses.

These features are depicted at least within figures 1 and 5 of the specification as originally filed. Nevertheless, these

features are not found within Carrender, Katayama and Kawana, either individually or as a whole.

Specifically, Carrender fails to disclose, teach or suggest the use of a received signal to generate a clock signal and a sampling signal, ***as claimed***.

For example, figure 1 of Carrender arguably teaches an identification system that produces first and second plurality of signal cycles (column 3, lines 27-35), but fails to disclose, teach or suggest the generation of a clock signal, and also fails to disclose, teach or suggest the generation of a sampling signal.

Figure 2 of Carrender arguably teaches the existence of controller 210 that supplies a clock signal (column 10, line 4), but fails to disclose, teach or suggest the use of a received signal to generate the clock signal.

Figure 5 of Carrender arguably teaches the presence of received data RX DATA (column 7, lines 62-65), but fails to teach the use of a received signal to generate the clock signal.

The Final Office Action contends that column 4, lines 10-43 of Carrender teaches the existence of a plurality of pulses formed during each cycle of the clock signal. But as noted hereinabove, the generation of a clock signal as claimed is not found within Carrender. Instead, the passage cited within the Final Office Action merely teaches first and second plurality of signal cycles (column 4, lines 18-20).

The Advisory Action of February 10, 2003 contends that Carrender teaches the generation of a clock signal **from the controller 210** (column 10, lines 1-5) by disclosing an antenna 206 to transmit and receive RF signal, an receiver 204 to receive the signal (column 4, lines 34-36), which is then processed by the signal processor and onto the controller 210 for the generation of a clock signal. Please note that the controller 210 is not the received signal, as claimed.

Again, please note that within claim 13 *the clock generation circuit uses a received signal to generate a clock signal and a sampling signal*. But as shown hereinabove, Carrender fails to disclose, teach or suggest a clock generation circuit that uses a received signal to generate a clock signal and a sampling signal.

Further note that figures 13, 15, 16, 20, 22 and 24 of Katayama fail to disclose, teach or suggest a plurality of logic levels generated during each cycle of the clock signal, wherein a logic level of the plurality of logic levels is the signal level of the received signal when sampled by a pulse of the plurality of pulses, as claimed.

While Kawana arguably teaches an IC card system, Kawana fails to disclose, teach or suggest the above-noted features deficient within Carrender and Katayama. For example, the use of a received signal to generate a clock signal and a sampling signal or a plurality of logic levels generated during each cycle of the clock signal are not found within Kawana.

Claim 14

The rejection of this claim respectfully traversed, at least for reasons provided hereinabove regarding claim 13 and at least for the following reasons.

Within claim 14, the phase of the clock signal is compared to the phase of the received signal. The clock signal, when out of phase with the received signal, is brought into phase with the received signal.

The feature of clock signal, when out of phase with the received signal, being brought into phase with the received signal is not found within Carrender, either expressly or impliedly. Instead, Carrender arguably teaches that each channel is approximately 90 degrees out of phase from the other (column 9, lines 2-3). Katayama and Kawana are silent as to the features absent within Carrender.

Claim 15

The rejection of this claim respectfully traversed, at least for reasons provided hereinabove regarding claim 13 and at least for the following reasons.

Within claim 15, the decoder includes a storage medium. The plurality of logic levels is used to address a storage medium location within the storage medium. The received data is stored at the storage medium location.

Carrender arguably teaches memory 212. However, Carrender fails to disclose, teach or suggest a ***plurality of logic levels*** being generated during the each cycle of the clock signal, as claimed within parent claim 13.

Moreover, Carrender fails to disclose, teach or suggest the plurality of logic levels being used to address a storage medium location within memory 212.

Katayama and Kawana are silent as to the features absent within Carrender.

Claim 18, 21

Claim 18 and the claims dependent thereon are drawn to an IC card for receiving data transmitted by a reader/writer and for outputting data from an internal memory in return, the IC card comprising:

a clock generation circuit, the clock generation circuit using a received signal to generate a clock signal and a sampling signal,

received data being the information transmitted to the IC card by way of the received signal,

the sampling signal having a plurality of pulses during each cycle of the clock signal,

a plurality of logic levels being generated during the each cycle of the clock signal,

a logic level of the plurality of logic levels being the signal level of the received signal when sampled by a pulse of the plurality of pulses; and

a decoder, the decoder decoding the plurality of logic levels to generate the received data.

These features are depicted at least within figures 1 and 5 of the specification as originally filed. Nevertheless, these features are not found within Carrender, Katayama and Kawana, either individually or as a whole.

Specifically, Carrender fails to disclose, teach or suggest the use of a received signal to generate a clock signal and a sampling signal, ***as claimed***.

For example, figure 1 of Carrender arguably teaches an identification system that produces first and second plurality of signal cycles (column 3, lines 27-35), but fails to disclose,

teach or suggest the generation of a clock signal, and also fails to disclose, teach or suggest the generation of a sampling signal.

Figure 2 of Carrender arguably teaches the existence of controller 210 that supplies a clock signal (column 10, line 4), but fails to disclose, teach or suggest the use of a received signal to generate the clock signal.

Figure 5 of Carrender arguably teaches the presence of received data RX DATA (column 7, lines 62-65), but fails to teach the use of a received signal to generate the clock signal.

The Final Office Action contends that column 4, lines 10-43 of Carrender teaches the existence of a plurality of pulses formed during each cycle of the clock signal. But as noted hereinabove, the generation of a clock signal as claimed is not found within Carrender. Instead, the passage cited within the Final Office Action merely teaches first and second plurality of signal cycles (column 4, lines 18-20).

The Advisory Action of February 10, 2003 contends that Carrender teaches the generation of a clock signal **from the**

controller 210 (column 10, lines 1-5) by disclosing an antenna 206 to transmit and receive RF signal, an receiver 204 to receive the signal (column 4, lines 34-36), which is then processed by the signal processor and onto the controller 210 for the generation of a clock signal. Please note that the controller 210 is not the received signal, as claimed.

Again, please note that within claim 13 *the clock generation circuit uses a received signal to generate a clock signal and a sampling signal*. But as shown hereinabove, Carrender fails to disclose, teach or suggest a clock generation circuit that uses a received signal to generate a clock signal and a sampling signal.

Further note that figures 13, 15, 16, 20, 22 and 24 of Katayama fail to disclose, teach or suggest a plurality of logic levels generated during each cycle of the clock signal, wherein a logic level of the plurality of logic levels is the signal level of the received signal when sampled by a pulse of the plurality of pulses, as claimed.

While Kawana arguably teaches an IC card system, Kawana fails to disclose, teach or suggest the above-noted features deficient within Carrender and Katayama. For example, the use of

a received signal to generate a clock signal and a sampling signal or a plurality of logic levels generated during each cycle of the clock signal are not found within Kawana.

Claim 19

The rejection of this claim respectfully traversed, at least for reasons provided hereinabove regarding claim 18 and at least for the following reasons.

Within claim 19, the phase of the clock signal is compared to the phase of the received signal. The clock signal, when out of phase with the received signal, is brought into phase with the received signal.

The feature of clock signal, when out of phase with the received signal, being brought into phase with the received signal is not found within Carrender, either expressly or impliedly. Instead, Carrender arguably teaches that each channel is approximately 90 degrees out of phase from the other (column 9, lines 2-3). Katayama and Kawana are silent as to the features absent within Carrender.

Claim 20

The rejection of this claim respectfully traversed, at least for reasons provided hereinabove regarding claim 18 and at least for the following reasons.

Within claim 20, the decoder includes a storage medium. The plurality of logic levels is used to address a storage medium location within the storage medium. The received data is stored at the storage medium location.

Carrender arguably teaches memory 212. However, Carrender fails to disclose, teach or suggest a ***plurality of logic levels*** being generated during the each cycle of the clock signal, as claimed within parent claim 18.

Moreover, Carrender fails to disclose, teach or suggest the plurality of logic levels being used to address a storage medium location within memory 212.

Claim 22, 25

Claim 22 and the claims dependent thereon are drawn to a reader/writer for receiving data transmitted by an IC card, the reader/writer comprising:

a clock generation circuit, the clock generation circuit using a received signal to generate a clock signal and a sampling signal,

received data being the information transmitted to the reader/writer by way of the received signal,

the sampling signal having a plurality of pulses during each cycle of the clock signal,

a plurality of logic levels being generated during the each cycle of the clock signal,

a logic level of the plurality of logic levels being the signal level of the received signal when sampled by a pulse of the plurality of pulses; and

a decoder, the decoder decoding the plurality of logic levels to generate the received data.

These features are depicted at least within figures 1 and 5 of the specification as originally filed. Nevertheless, these

features are not found within Carrender, Katayama and Kawana, either individually or as a whole.

Specifically, Carrender fails to disclose, teach or suggest the use of a received signal to generate a clock signal and a sampling signal, ***as claimed***.

For example, figure 1 of Carrender arguably teaches an identification system that produces first and second plurality of signal cycles (column 3, lines 27-35), but fails to disclose, teach or suggest the generation of a clock signal, and also fails to disclose, teach or suggest the generation of a sampling signal.

Figure 2 of Carrender arguably teaches the existence of controller 210 that supplies a clock signal (column 10, line 4), but fails to disclose, teach or suggest the use of a received signal to generate the clock signal.

Figure 5 of Carrender arguably teaches the presence of received data RX DATA (column 7, lines 62-65), but fails to teach the use of a received signal to generate the clock signal.

The Final Office Action contends that column 4, lines 10-43 of Carrender teaches the existence of a plurality of pulses formed during each cycle of the clock signal. But as noted hereinabove, the generation of a clock signal as claimed is not found within Carrender. Instead, the passage cited within the Final Office Action merely teaches first and second plurality of signal cycles (column 4, lines 18-20).

The Advisory Action of February 10, 2003 contends that Carrender teaches the generation of a clock signal **from the controller 210** (column 10, lines 1-5) by disclosing an antenna 206 to transmit and receive RF signal, an receiver 204 to receive the signal (column 4, lines 34-36), which is then processed by the signal processor and onto the controller 210 for the generation of a clock signal. Please note that the controller 210 is not the received signal, as claimed.

Again, please note that within claim 13 *the clock generation circuit uses a received signal to generate a clock signal and a sampling signal*. But as shown hereinabove, Carrender fails to disclose, teach or suggest a clock generation circuit that uses a received signal to generate a clock signal and a sampling signal.

Further note that figures 13, 15, 16, 20, 22 and 24 of Katayama fail to disclose, teach or suggest a plurality of logic levels generated during each cycle of the clock signal, wherein a logic level of the plurality of logic levels is the signal level of the received signal when sampled by a pulse of the plurality of pulses, as claimed.

While Kawana arguably teaches an IC card system, Kawana fails to disclose, teach or suggest the above-noted features deficient within Carrender and Katayama. For example, the use of a received signal to generate a clock signal and a sampling signal or a plurality of logic levels generated during each cycle of the clock signal are not found within Kawana.

Claim 23

The rejection of this claim respectfully traversed, at least for reasons provided hereinabove regarding claim 22 and at least for the following reasons.

Within claim 23, the phase of the clock signal is compared to the phase of the received signal. The clock signal, when out of phase with the received signal, is brought into phase with the received signal.

The feature of clock signal, when out of phase with the received signal, being brought into phase with the received signal is not found within Carrender, either expressly or impliedly. Instead, Carrender arguably teaches that each channel is approximately 90 degrees out of phase from the other (column 9, lines 2-3). Katayama and Kawana are silent as to the features absent within Carrender.

Claim 24

The rejection of this claim respectfully traversed, at least for reasons provided hereinabove regarding claim 22 and at least for the following reasons.

Within claim 24, the decoder includes a storage medium. The plurality of logic levels is used to address a storage medium location within the storage medium. The received data is stored at the storage medium location.

Carrender arguably teaches memory 212. However, Carrender fails to disclose, teach or suggest a ***plurality of logic levels*** being generated during the each cycle of the clock signal, as claimed within parent claim 22.

Moreover, Carrender fails to disclose, teach or suggest the plurality of logic levels being used to address a storage medium location within memory 212.

Katayama and Kawana are silent as to the features absent within Carrender.

The Examiner erred in rejecting claims 26-37 under 35 U.S.C. §103 as allegedly being obvious over Carrender in view of Kurihara.

This rejection is respectfully traversed, at least for the following reasons.

Claim 26

Claim 26 and the claims dependent thereon are drawn to a portable electronic apparatus comprising:

a clock generation circuit, the clock generation circuit using a received signal to generate a clock signal,

received data being the information transmitted to the portable electronic apparatus by way of the received signal; and

a correlation value detection circuit, the correlation value detection circuit comparing the phase of the clock signal to the phase of the received signal to generate a correlation value signal,

the correlation value signal trending in a first direction when the clock signal is in phase with the received signal and trending in a direction opposite to the first direction when the clock signal is out of phase with the received signal;

a determination circuit, the determination circuit using the correlation value signal to generate the received data.

Within claim 26, a received signal is used to generate a clock signal. In addition, the correlation value detection circuit compares the phase of the clock signal to the phase of the received signal to generate a correlation value signal, wherein the correlation value signal trends in a first direction

when the clock signal is in phase with the received signal and trends in a direction opposite to the first direction when the clock signal is out of phase with the received signal. These features are explained at least within figures 6 and 10 of the specification as originally filed. Yet, these features are not found within Carrender and Kurihara, either individually or as a whole.

In particular, failings in the teaching of Carrender have been noted hereinabove. In particular, Carrender fails to disclose, teach or suggest the use of a received signal to generate a clock signal and a sampling signal, as claimed.

For example, figure 1 of Carrender arguably teaches an identification system that produces first and second plurality of signal cycles (column 3, lines 27-35), but fails to disclose, teach or suggest the generation of a clock signal, and also fails to disclose, teach or suggest the generation of a sampling signal.

Figure 2 of Carrender arguably teaches the existence of controller 210 that supplies a clock signal (column 10, line 4), but fails to disclose, teach or suggest the use of a received

signal to generate the clock signal.

Figure 5 of Carrender arguably teaches the presence of received data RX DATA (column 7, lines 62-65), but fails to teach the use of a received signal to generate the clock signal.

In addition, Carrender fails to disclose, teach or suggest the correlation value detection circuit comparing the phase of the clock signal to the phase of the received signal to generate a correlation value signal.

While Kurihara arguably teaches a sliding correlator, Kurihara fails to disclose, teach or suggest a comparison of phase of the clock signal to the phase of the received signal to generate a correlation value signal.

Instead, figures 2, 3 of Kurihara arguably depict input signal as a delayed input signal OUTPUT 1 and further depicts input signal as an non-delayed input signal OUTPUT 2 that are multiplied by multipliers 12, 13 and compared by comparator 16, but fails to disclose, teach or suggest a comparison of phase of the clock signal to the phase of the received signal to generate a correlation value signal, as claimed.

Figure 4 of Kurihara arguably depicts input signal as a digitized input signal from correlating unit 27 and further depicts a digitized input signal from correlating unit 28 (column 7, lines 48-49). While figure 4 depict clock generator 32, figure 4 fails to disclose, teach or suggest the use of a received signal to generate a clock signal, as claimed.

Claim 27

The rejection of this claim respectfully traversed, at least for reasons provided hereinabove regarding claim 26 and at least for the following reasons.

Within claim 27, a value of the correlation value signal establishes the logic level of the received data, the logic level being one of a "0" logic level and a "1" logic level.

However, Carrender and Kurihara fail to disclose, teach or suggest the correlation value detection circuit comparing the phase of the clock signal to the phase of the received signal to generate a correlation value signal.

Claim 28

The rejection of this claim respectfully traversed, at least for reasons provided hereinabove regarding claim 26 and at least for the following reasons.

Within the parent claim, the correlation value signal trends in a first direction when the clock signal is in phase with the received signal and trends in a direction opposite to the first direction when the clock signal is out of phase with the received signal. Within claim 28, the first direction is an increasing direction and the direction opposite to the first direction is a decreasing direction.

However, Carrender and Kurihara fail to disclose, teach or suggest the first direction is an increasing direction and the direction opposite to the first direction is a decreasing direction.

Claim 29

The rejection of this claim respectfully traversed, at least for reasons provided hereinabove regarding claim 26 and at least for the following reasons.

Within claim 26, the correlation value detection circuit compares the phase of the clock signal to the phase of the received signal to generate a correlation value signal. Within claim 29, the correlation value signal is bounded by a maximum amount and a minimum amount, the minimum amount being less than the maximum amount.

However, Carrender and Kurihara fail to disclose, teach or suggest the correlation value signal being bounded by a maximum amount and a minimum amount, the minimum amount being less than the maximum amount.

Claim 30

Claim 30 and the claims dependent thereon are drawn to an IC card for receiving data transmitted by a reader/writer and for outputting data from an internal memory in return, the IC card comprising:

a clock generation circuit, the clock generation circuit using a received signal to generate a clock signal,

received data being the information transmitted to the IC card by way of the received signal; and

a correlation value detection circuit, the correlation value detection circuit comparing the phase of the clock signal to the phase of the received signal to generate a correlation value signal,

the correlation value signal trending in a first direction when the clock signal is in phase with the received signal and trending in a direction opposite to the first direction when the clock signal is out of phase with the received signal;

a determination circuit, the determination circuit using the correlation value signal to generate the received data.

Within claim 30, a received signal is used to generate a clock signal. In addition, the correlation value detection circuit compares the phase of the clock signal to the phase of the received signal to generate a correlation value signal, wherein the correlation value signal trends in a first direction when the clock signal is in phase with the received signal and trends in a direction opposite to the first direction when the clock signal is out of phase with the received signal. These

features are explained at least within figures 6 and 10 of the specification as originally filed. Yet, these features are not found within Carrender and Kurihara, either individually or as a whole.

In particular, failings in the teaching of Carrender have been noted hereinabove. In particular, Carrender fails to disclose, teach or suggest the use of a received signal to generate a clock signal and a sampling signal, as claimed.

For example, figure 1 of Carrender arguably teaches an identification system that produces first and second plurality of signal cycles (column 3, lines 27-35), but fails to disclose, teach or suggest the generation of a clock signal, and also fails to disclose, teach or suggest the generation of a sampling signal.

Figure 2 of Carrender arguably teaches the existence of controller 210 that supplies a clock signal (column 10, line 4), but fails to disclose, teach or suggest the use of a received signal to generate the clock signal.

Figure 5 of Carrender arguably teaches the presence of

received data RX DATA (column 7, lines 62-65), but fails to teach the use of a received signal to generate the clock signal.

In addition, Carrender fails to disclose, teach or suggest the correlation value detection circuit comparing the phase of the clock signal to the phase of the received signal to generate a correlation value signal.

While Kurihara arguably teaches a sliding correlator, Kurihara fails to disclose, teach or suggest a comparison of phase of the clock signal to the phase of the received signal to generate a correlation value signal.

Instead, figures 2, 3 of Kurihara arguably depict input signal as a delayed input signal OUTPUT 1 and further depicts input signal as an non-delayed input signal OUTPUT 2 that are multiplied by multipliers 12, 13 and compared by comparator 16, but fails to disclose, teach or suggest a comparison of phase of the clock signal to the phase of the received signal to generate a correlation value signal, as claimed.

Figure 4 of Kurihara arguably depicts input signal as a digitized input signal from correlating unit 27 and further

depicts a digitized input signal from correlating unit 28 (column 7, lines 48-49). While figure 4 depict clock generator 32, figure 4 fails to disclose, teach or suggest the use of a received signal to generate a clock signal, as claimed.

Claim 31

The rejection of this claim respectfully traversed, at least for reasons provided hereinabove regarding claim 30 and at least for the following reasons.

Within claim 31, a value of the correlation value signal establishes the logic level of the received data, the logic level being one of a "0" logic level and a "1" logic level.

However, Carrender and Kurihara fail to disclose, teach or suggest the correlation value detection circuit comparing the phase of the clock signal to the phase of the received signal to generate a correlation value signal.

Claim 32

The rejection of this claim respectfully traversed, at least for reasons provided hereinabove regarding claim 30 and at least for the following reasons.

Within claim 32, the first direction is an increasing direction and the direction opposite to the first direction is a decreasing direction.

Claim 33

The rejection of this claim respectfully traversed, at least for reasons provided hereinabove regarding claim 30 and at least for the following reasons.

Within claim 30, the correlation value detection circuit compares the phase of the clock signal to the phase of the received signal to generate a correlation value signal. Within claim 33, the correlation value signal is bounded by a maximum amount and a minimum amount, the minimum amount being less than the maximum amount.

However, Carrender and Kurihara fail to disclose, teach or suggest the correlation value signal being bounded by a maximum amount and a minimum amount, the minimum amount being less than the maximum amount.

Claim 34

Claim 34 and the claims dependent thereon are drawn to an IC card, the reader/writer comprising:

a clock generation circuit, the clock generation circuit using a received signal to generate a clock signal,

received data being the information transmitted to the reader/writer by way of the received signal; and

a correlation value detection circuit, the correlation value detection circuit comparing the phase of the clock signal to the phase of the received signal to generate a correlation value signal,

the correlation value signal trending in a first direction when the clock signal is in phase with the received signal and trending in a direction opposite to the first direction when the clock signal is out of phase with the received signal;

a determination circuit, the determination circuit using the correlation value signal to generate the received data.

Within claim 34, a received signal is used to generate a clock signal. In addition, the correlation value detection circuit compares the phase of the clock signal to the phase of the received signal to generate a correlation value signal, wherein the correlation value signal trends in a first direction when the clock signal is in phase with the received signal and trends in a direction opposite to the first direction when the clock signal is out of phase with the received signal. These features are explained at least within figures 6 and 10 of the specification as originally filed. Yet, these features are not found within Carrender and Kurihara, either individually or as a whole.

In particular, failings in the teaching of Carrender have been noted hereinabove. In particular, Carrender fails to disclose, teach or suggest the use of a received signal to generate a clock signal and a sampling signal, as claimed.

For example, figure 1 of Carrender arguably teaches an identification system that produces first and second plurality of signal cycles (column 3, lines 27-35), but fails to disclose, teach or suggest the generation of a clock signal, and also fails

to disclose, teach or suggest the generation of a sampling signal.

Figure 2 of Carrender arguably teaches the existence of controller 210 that supplies a clock signal (column 10, line 4), but fails to disclose, teach or suggest the use of a received signal to generate the clock signal.

Figure 5 of Carrender arguably teaches the presence of received data RX DATA (column 7, lines 62-65), but fails to teach the use of a received signal to generate the clock signal.

In addition, Carrender fails to disclose, teach or suggest the correlation value detection circuit comparing the phase of the clock signal to the phase of the received signal to generate a correlation value signal.

While Kurihara arguably teaches a sliding correlator, Kurihara fails to disclose, teach or suggest a comparison of phase of the clock signal to the phase of the received signal to generate a correlation value signal.

Instead, figures 2, 3 of Kurihara arguably depict input

signal as a delayed input signal OUTPUT 1 and further depicts input signal as an non-delayed input signal OUTPUT 2 that are multiplied by multipliers 12, 13 and compared by comparator 16, but fails to disclose, teach or suggest a comparison of phase of the clock signal to the phase of the received signal to generate a correlation value signal, as claimed.

Figure 4 of Kurihara arguably depicts input signal as a digitized input signal from correlating unit 27 and further depicts a digitized input signal from correlating unit 28 (column 7, lines 48-49). While figure 4 depict clock generator 32, figure 4 fails to disclose, teach or suggest the use of a received signal to generate a clock signal, as claimed.

Claim 35

The rejection of this claim respectfully traversed, at least for reasons provided hereinabove regarding claim 26 and at least for the following reasons.

Within claim 35, a value of the correlation value signal establishes the logic level of the received data, the logic level being one of a "0" logic level and a "1" logic level.

However, Carrender and Kurihara fail to disclose, teach or suggest the correlation value detection circuit comparing the phase of the clock signal to the phase of the received signal to generate a correlation value signal.

Claim 36

The rejection of this claim respectfully traversed, at least for reasons provided hereinabove regarding claim 26 and at least for the following reasons.

Within claim 34, the correlation value detection circuit compares the phase of the clock signal to the phase of the received signal to generate a correlation value signal. Within claim 36, the correlation value signal is bounded by a maximum amount and a minimum amount, the minimum amount being less than the maximum amount.

However, Carrender and Kurihara fail to disclose, teach or suggest the correlation value signal being bounded by a maximum amount and a minimum amount, the minimum amount being less than the maximum amount.

Claim 37

The rejection of this claim respectfully traversed, at least for reasons provided hereinabove regarding claim 34 and at least for the following reasons.

Within claim 34, the correlation value detection circuit compares the phase of the clock signal to the phase of the received signal to generate a correlation value signal. Within claim 37, the correlation value signal is bounded by a maximum amount and a minimum amount, the minimum amount being less than the maximum amount.

However, Carrender and Kurihara fail to disclose, teach or suggest the correlation value signal being bounded by a maximum amount and a minimum amount, the minimum amount being less than the maximum amount.

X. Conclusion

Carrender, Katayama, Kawana, and Kurihara, either individually or as a whole, fail to disclose, teach or suggest all the components of claims 13-37. As a result, Carrender, Katayama, Kawana, and Kurihara fail to render Applicant's invention obvious. The claims are considered allowable for the

reasons discussed above, as well as for the additional features they recite.

Because Applicant submits that the Examiner's basis for making the final rejection of claims 13-37 is both improper and unreasonable, withdrawal of this rejection is respectfully requested.

In view of the foregoing, it is submitted that the final rejection of claims 13-37 is improper and should not be sustained. Therefore, a reversal of the Final Rejection of November 7, 2002 as to claims 13-37 is respectfully requested.

Respectfully submitted,

DATE: May 5, 2003

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XI. APPENDIX

Claims on Appeal

13. A portable electronic apparatus comprising:

a clock generation circuit, said clock generation circuit using a received signal to generate a clock signal and a sampling signal,

received data being the information transmitted to said portable electronic apparatus by way of said received signal,

said sampling signal having a plurality of pulses during each cycle of said clock signal,

a plurality of logic levels being generated during said each cycle of said clock signal,

a logic level of said plurality of logic levels being the signal level of said received signal when sampled by a pulse of said plurality of pulses; and

a decoder, said decoder decoding said plurality of logic levels to generate said received data.

14. The portable electronic apparatus according to claim 13, wherein the phase of said clock signal is compared to the phase of said received signal,

said clock signal, when out of phase with said received signal, is brought into phase with said received signal.

15. The portable electronic apparatus according to claim 13, wherein said decoder includes a storage medium,

said plurality of logic levels being used to address a storage medium location within said storage medium,

said received data being stored at said storage medium location.

16. The portable electronic apparatus according to claim 13, wherein said received signal is wirelessly transmitted to said portable electronic apparatus.

17. The portable electronic apparatus according to claim 16, wherein said received signal is a modulated signal.

18. An IC card for receiving data transmitted by a reader/writer and for outputting data from an internal memory in return, said IC card comprising:

a clock generation circuit, said clock generation circuit using a received signal to generate a clock signal and a sampling signal,

received data being the information transmitted to said IC card by way of said received signal,

said sampling signal having a plurality of pulses during each cycle of said clock signal,

a plurality of logic levels being generated during said each cycle of said clock signal,

a logic level of said plurality of logic levels being the signal level of said received signal when sampled by a pulse of said plurality of pulses; and

a decoder, said decoder decoding said plurality of logic levels to generate said received data.

19. The IC card according to claim 18, wherein the phase of said clock signal is compared to the phase of said received signal,

said clock signal, when out of phase with said received signal, is brought into phase with said received signal.

20. The IC card according to claim 18, wherein said decoder includes a storage medium,

said plurality of logic levels being used to address a storage medium location within said storage medium,

said received data being stored at said storage medium location.

21. The IC card according to claim 18, wherein said received signal is wirelessly transmitted to said portable electronic apparatus.

22. A reader/writer for receiving data transmitted by an IC card, said reader/writer comprising:

a clock generation circuit, said clock generation circuit using a received signal to generate a clock signal and a sampling signal,

received data being the information transmitted to said reader/writer by way of said received signal,

said sampling signal having a plurality of pulses during each cycle of said clock signal,

a plurality of logic levels being generated during said each cycle of said clock signal,

a logic level of said plurality of logic levels being the signal level of said received signal when sampled by a pulse of said plurality of pulses; and

a decoder, said decoder decoding said plurality of logic levels to generate said received data.

23. The reader/writer according to claim 22, wherein the phase of said clock signal is compared to the phase of said received signal,

said clock signal, when out of phase with said received signal, is brought into phase with said received signal.

24. The reader/writer according to claim 22, wherein said decoder includes a storage medium,

said plurality of logic levels being used to address a storage medium location within said storage medium,

said received data being stored at said storage medium location.

25. The reader/writer according to claim 22, wherein said received signal is wirelessly transmitted to said portable electronic apparatus.

26. A portable electronic apparatus comprising:

a clock generation circuit, said clock generation circuit using a received signal to generate a clock signal,

received data being the information transmitted to said portable electronic apparatus by way of said received signal; and

a correlation value detection circuit, said correlation value detection circuit comparing the phase of said clock signal to the phase of said received signal to generate a correlation value signal,

said correlation value signal trending in a first direction when said clock signal is in phase with said received signal and trending in a direction opposite to said first direction when said clock signal is out of phase with said received signal;

a determination circuit, said determination circuit using said correlation value signal to generate said received data.

27. The portable electronic apparatus according to claim 26, wherein a value of said correlation value signal establishes the logic level of said received data, said logic level being one of a "0" logic level and a "1" logic level.

28. The portable electronic apparatus according to claim 26, wherein said first direction is an increasing direction and said

direction opposite to said first direction is a decreasing direction.

29. The portable electronic apparatus according to claim 26, wherein said correlation value signal is bounded by a maximum amount and a minimum amount, said minimum amount being less than said maximum amount.

30. An IC card for receiving data transmitted by a reader/writer and for outputting data from an internal memory in return, said IC card comprising:

a clock generation circuit, said clock generation circuit using a received signal to generate a clock signal,

received data being the information transmitted to said IC card by way of said received signal; and

a correlation value detection circuit, said correlation value detection circuit comparing the phase of said clock signal to the phase of said received signal to generate a correlation value signal,

said correlation value signal trending in a first direction when said clock signal is in phase with said received signal and trending in a direction opposite to said

first direction when said clock signal is out of phase with said received signal;

a determination circuit, said determination circuit using said correlation value signal to generate said received data.

31. The IC card according to claim 30, wherein a value of said correlation value signal establishes the logic level of said received data, said logic level being one of a "0" logic level and a "1" logic level.

32. The IC card according to claim 30, wherein said first direction is an increasing direction and said direction opposite to said first direction is a decreasing direction.

33. An IC card according to claim 30, wherein said correlation value signal is bounded by a maximum amount and a minimum amount, said minimum amount being less than said maximum amount.

34. A reader/writer for receiving data transmitted by an IC card, said reader/writer comprising:

a clock generation circuit, said clock generation circuit using a received signal to generate a clock signal,

received data being the information transmitted to said reader/writer by way of said received signal; and

a correlation value detection circuit, said correlation value detection circuit comparing the phase of said clock signal to the phase of said received signal to generate a correlation value signal,

said correlation value signal trending in a first direction when said clock signal is in phase with said received signal and trending in a direction opposite to said first direction when said clock signal is out of phase with said received signal;

a determination circuit, said determination circuit using said correlation value signal to generate said received data.

35. The reader/writer according to claim 34, wherein a value of said correlation value signal establishes the logic level of said received data, said logic level being one of a "0" logic level and a "1" logic level.

36. The reader/writer according to claim 34, wherein said first direction is an increasing direction and said direction opposite to said first direction is a decreasing direction.

37. The reader/writer according to claim 34, wherein said correlation value signal is bounded by a maximum amount and a minimum amount, said minimum amount being less than said maximum amount.